WHAT IS CLAIMED IS:

1. A data transfer controller comprising:

an initial value register, a transfer start address of a transfer source or transfer destination being initially set to said initial value register from an external; and

a control unit which requests an interrupt to the external each time data transfer responding to a transfer request from the external reaches a predetermined data amount based upon the transfer start address, and initializes an address of the transfer source or transfer destination to the transfer start address in said initial value register each time the interrupt is issued a plurality of predetermined times.

2. A data processor comprising an arithmetic and logic controller and a data transfer controller formed on a semiconductor chip, wherein said arithmetic and logic controller initially sets a transfer start address of a transfer source of transfer destination to said data transfer controller, and said data transfer controller requests an interrupt to said arithmetic and logic controller each time data transfer responding to a transfer request from the transfer source reaches a predetermined data amount based upon the transfer start address, and initializes an address of the transfer source or transfer destination to the transfer start address each time the interrupt is issued a plurality of predetermined times.

3. A data processing system comprising an arithmetic and logic controller, a data transfer controller whose transfer control conditions are set by said arithmetic and logic controller, a RAM accessible by said arithmetic and logic controller and said data transfer controller, and a peripheral circuit which issues a transfer request to said data transfer controller, wherein:

said data transfer controller requests an interrupt to said arithmetic and logic controller each time data transfer to said RAM responding to a transfer request from the said peripheral circuit reaches a predetermined data amount based upon a transfer start address of said RAM indicated by the transfer control conditions set by said arithmetic and logic controller, and initializes an address of the transfer source or transfer destination to the transfer start address each time the interrupt is issued a plurality of predetermined times; and

after the interrupt from said data transfer controller is acknowledged, said arithmetic and logic controller reads data transferred to said RAM before the interrupt is issued, and performs data processing.

4. A data transfer controller comprising:

an initial value register capable of being externally set with transfer control address information;

an address counting unit which renews the

transfer control address information each time data is transferred from a transfer source to a transfer destination;

a temporary address register to which the transfer control address information set to said initial value register is set, the set transfer control address information being sequentially renewed by said address counting means;

a transfer number counting unit capable of repetitively performing an operation of counting the number of transfer times up to a first target number each time data is transferred from the transfer source to the transfer destination;

a repetition number counting unit capable of repetitively performing an operation of counting the number of repetition times of the operation of said transfer number counting unit which counts the number of transfer times up to the first target number, up to a second target number; and

a control unit which starts a data transfer operation from the transfer source to the transfer destination in response to a data transfer request, outputting an interrupt signal each time said transfer number counting unit counts the first target number, and setting the transfer control address information to said temporary register from said initial value register each time said repetition number counting unit counts the second target number.

5. A data transfer controller according to claim 4, wherein:

said temporary address register is a destination address register for storing a transfer destination address;

said initial value register is an initial address register to which a start address of the transfer destination is set; and

said control unit is capable of starting a data transfer control of storing data at the transfer source address in the transfer destination at a transfer destination address in the destination address register, in response to the data transfer request.

6. A data transfer controller according to claim 4, wherein:

said temporary address register is a source address register for storing a transfer source address;

said initial value register is an initial address register to which a start address of the transfer source is set; and

said control unit is capable of starting a data transfer control of storing data at the transfer source address in the source address register in the transfer destination at a transfer destination address, in response to the data transfer request.

7. A data transfer controller according to claim 4, further comprising a source address register for storing a transfer source address and a destination

register for storing a transfer destination address, wherein:

said control unit can select either said source address register or said destination address register as said temporary address register and can start a data transfer control by using the register selected as said temporary register, in response to the data transfer request.

8. A data transfer controller according to any one of claim 4, further comprising a transfer number designation register capable of being externally set with the first target number.

9. A data transfer controller according to any one of claim 4, wherein the second target number is three.

10. A data transfer controller according to any one of claim 1, further comprising a RAM usable as the transfer source or the transfer destination.

11. A data transfer controller comprising:

a plurality of initial value registers each capable of being externally set with transfer control address information;

an address counting circuit which renews the transfer control address information each time data is transferred from a transfer source to a transfer destination;

a selecting circuit capable of selecting the transfer control address information stored in one of a

plurality of said initial value registers;

a temporary address register to which the transfer control address information selected by said selecting circuit is set, the set transfer control address information being sequentially renewed by said address counting circuit;

transfer number counting circuit capable of repetitively performing an operation of counting the number of transfer times up to a first target number each time data is transferred from the transfer source to the transfer destination;

a repetition number counting circuit capable of repetitively performing an operation of counting the number of repetition times of the operation of said transfer number counting circuit which counts the number of transfer times up to the first target number, up to a second target number; and

a control circuit which starts a data transfer operation from the transfer source to the transfer destination in response to a data transfer request, outputs an interrupt signal each time said transfer number counting means counts the first target number, makes said selecting circuit select said initial value register in accordance with a count of said repetition number counting circuit, and sets the transfer control address information in the selected initial register to said temporary register.

12. A data processor comprising an arithmetic and

logic controller and a data transfer controller to which transfer control conditions are set by said arithmetic and logic controller, wherein said data transfer controller comprises:

an initial value register capable of being set with transfer control address information by said arithmetic and logic controller;

an address counting circuit which renews the transfer control address information each time data is transferred from a transfer source to a transfer destination;

a temporary address register to which the transfer control address information set to said initial value register is set, the set transfer control address information being sequentially renewed by said address counting means;

a transfer number counting circuit capable of repetitively performing an operation of counting the number of transfer times up to a first target number each time data is transferred from the transfer source to the transfer destination;

a repetition number counting circuit capable of repetitively performing an operation of counting the number of repetition times of the operation of said transfer number counting circuit for counting the number of transfer times up to the first target number, up to a second target number; and

a control circuit which starts a data

transfer operation from the transfer source to the transfer destination in response to a data transfer request, outputs an interrupt signal each time said transfer number counting circuit counts the first target number, and sets the transfer control address information in the initial register to said temporary register.

13. A data processor according to claim 12, further comprising a RAM accessible by said arithmetic and logic controller and said data transfer controller, said arithmetic and logic controller, said data transfer controller and said RAM being formed in a single semiconductor chip.

14. A data processor according to claim 13, further comprising a peripheral input/output circuit accessible by said arithmetic and logic controller and said data transfer controller, said peripheral input/output circuit being capable of outputting the data transfer request to said data transfer controller.

15. A data processing system comprising a data processor recited in claim 14 and a voice signal input circuit connected to said peripheral input/output circuit of the data processor, wherein:

the data processor stores an operation program for said arithmetic and logic controller;

in accordance with the operation program, said arithmetic and logic controller sets transfer conditions to said data transfer controller, the

transfer conditions being used when a voice signal input from said voice signal input circuit to said peripheral input/output circuit is transferred to said RAM;

said data transfer controller controls to transfer the voice signal to said RAM in response to the data transfer request from said peripheral input/output circuit; and

when an interrupt signal is received from said data transfer controller, said arithmetic and logic controller read the voice signal from said RAM and processes the read voice signal.